Register No.: 

# 2242

## October 2024

*Time – Three hours*
*(Maximum Marks: 100)*

*[N.B.* 1. Answer all questions under Part-A. Each question carries 3 marks.

2. Answer all the questions either (A) or (B) in Part-B. Each question carries 14 marks.]

## PART – A

1. Draw NOT gate using CMOS.
2. Define routing.
3. Write the syntax for process statement.
4. Give an example for if else statement.
5. Write the truth table for single bit comparator.
6. Write short notes on 2 to 4 decoder.
7. Define D flip-flop.
8. What is Johnson counter?
9. Write short notes on CPLD.
10. Write short notes on ASIC.

[Turn over.....

## PART – B

11. (a) Implement the function Y = (A+B) (C+D) using CMOS.

*(Or)*

(b) Write notes on design entry, simulation and synthesis in VLSI design process.

12. (a) Write a VHDL code for logic gates AND, OR and NOT.

*(Or)*

(b) Explain about case statement in VHDL with an example.

13. (a) Write a VHDL program for full adder and full subtractor.

*(Or)*

(b) Describe about 4 to 1 multiplexer.

14. (a) Write notes on JK flip flop.

*(Or)*

(b) Write a VHDL program for 3 bit up/down counter.

15. (a) Write notes on PROM, PLA and PAL.

*(Or)*

(b) Draw and explain the architecture of FPGA.

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